Amendments to the Specification

Please replace the Title with the following new Title:

Data Processing Device with Instruction Translator and Memory Interface Device to Translate Non-Native Instructions into Native Instructions for Processor

Please replace paragraph beginning on page 1, line 25 with the following amended paragraph:

One of the typical conventional schemes for executing the program written for the old processor on a new processor, is to provide hardware of the new processor with a function of the old processor. Referring to Fig. 1, a conventional data processing device [[500]] for performing such a method includes a processor 1 provided with a multifunction instruction decoder 5, which has functions of decoding both the instructions for the old processor and the instructions for the new processor, and an arithmetic portion 6 having a function of executing these instructions. ~~Data~~ The data processing device [[500]] further includes a bus 4 connected to processor 1 as well as a data memory 2 and an instruction memory 3, which are connected to bus 4.

Please replace paragraph beginning on page 9, line 28 with the following amended paragraph:

Control portion 532 determines whether the address value sent from MUX 531 falls within a predetermined address region, and controls selectors 535, 538 and 536 in accordance with the determination. This predetermined address region corresponds to an address region 537 in Fig. 13, which will be described later. When control portion 532 receives the address value falling within the predetermined address region, it controls selector 535 to select signal line 543

so that the address value on signal line 543, which is prepared by 3-bit right shift of the address value on signal line 542 by shift circuit 534, is output onto signal line 545. Otherwise, the control portion 532 controls selector 535 to select signal line 542 and output the address value on signal line 542 onto signal line 545. When control portion 532 receives the address value falling within the predetermined address region, it controls selector 536 to select signal line 539 and output the instruction on signal line 539 (i.e., the native instruction prepared by translating the nonnative instruction by translation circuit 540 [[539]]) onto signal line 104. Otherwise, control portion 532 controls selector 536 to select signal line 563 and output the instruction (native instruction) on signal line 541 onto signal line 105 [[104]]. When the control portion 532 receives the address value falling within the predetermined address region, it controls selector 538 to select signal line 544 and output the address value on signal line 544 onto signal line 31. Otherwise, it controls selector 538 to select signal line 545 and output the address value on signal line 545 onto signal line 31.